A Nonlinear Microwave MOSFET Model for Spice Simulators

Charlotte E. Biber, Martin L. Schmatz, Thomas Morf, *Member, IEEE,* Urs Lott, *Member, IEEE,* and Werner Bächtold

***Abstract*— As the gate lengths of silicon MOSFET's become smaller and smaller, these devices are usable to frequencies in the gigahertz range. The nonlinear MOSFET model presented in this paper is based on S-parameter measurements over a large bias range, and has been implemented in a SPICE simulator. The improvements consist of new equations for the nonlinear capacitances and output conductance of the MOS transistor. This new large-signal model shows very good agreement between measured and simulated S-parameters of single transistors at various bias points up to 10 GHz. Intermodulation (IM) and circuit performance are also well predicted. Simulated S-parameters of a simple amplifier showed excellent agreement with measured results, confirming the performance of this model.**

***Index Terms*— CMOS FR, high frequency, microwave modeling, modeling, MOSFET, silicon, SPICE.**

I. Introduction

SILICON-DEVICE technology has become an attractive low-cost solution for many high-frequency personal communication products [1]. These analog applications require good high-frequency models in the design phase in order to predict the RF circuit performance with accuracy. Though many MOS models exist, the most widely used models of the MOS transistor are not particularly suited for high frequencies [2].

The number of parameters required to fit such a model is rather large; BSIM1 [3] for example, requires more than 70 parameters for a complete model. Significant extraction experience or an automated extraction program such as ICCAP[1] is required to obtain model parameters in a reasonable time frame.

The ultimate goal in modeling is a versatile model with few parameters (less than 20) and good accuracy in all regions of operation. Much work has been done in the investigation of the dc performance of MOS models in all regions of operation [4], [5].[2] However, RF performance has not yet been investigated in such detail.

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[1] *ICCAP User's Manual*. Hewlett-Packard Co., Pasadena, CA, 1995.

[2] *BSIM3v3 Manual*, Dept. EECS, Univ. California, Berkeley, 1995.

A model modification to improve the RF performance of any existing dc model is presented. Based on S-parameter measurements, this model significantly improves the prediction of the high-frequency circuit performance.

The model modification presented in this paper proposes new equations for the nonlinear capacitances and the high-frequency output conductance of MOS transistors. To simplify the implementation, the dc drain current equation of the Enz–Krummenacher–Vittoz (EKV) [4], [5] model was used while the accuracy for RF simulations was achieved by adding new capacitance equations within the model program code. The combination of the dc and RF parts of the model predicts the nonlinear high-frequency performance up to 10 GHz over all operating bias points.

II. Modeling Process

In order to verify the proposed model improvements, test transistors on a CMOS process from Toshiba having a minimal gate length of 0.36 μm and a total gatewidth of 100 μm with 20 fingers were used. Small-signal on-wafer S-parameters have been measured for a transistor test structure at various bias points. These bias points ranged from 0.5 to 2.5 V for the gate–source voltage and 0.0 to 1.5 V for the drain–source voltage. The deembedding of the extrinsic structures (pads) is described in [6]. The small-signal intrinsic elements were determined by direct extraction from this deembedded data, as in [7]. The small-signal equivalent circuit used is shown in Fig. 1 [8].

The output conductance is modeled in two parts [9]: $1/R_{\rm ds}$ and the $1/Z_{\rm dsout}$. The $1/R_{\rm ds}$ models the low-frequency output conductance while the high-frequency output impedance is dominated by $C_{\rm ds1}$, $C_{\rm ds2}$ and $R_{\rm ds1}$, which combine to form $Z_{\rm dsout}$ (Fig. 1).

The total error (1) for all measured bias points between the measured and the extracted S-parameters of the new model is shown in Fig. 2. The error is calculated at each bias point and given in percent:

$$\varepsilon_{\rm tot} = 100 \cdot \frac{1}{4} \cdot \sum_{ij} \left\{ \sum_{\rm freq} \frac{|{\rm meas}S_{ij} - {\rm sim}S_{ij}|^2}{|{\rm meas}S_{ij}|^2} \right\} \frac{1}{N_{\rm freq}} \quad (1)$$

where ${\rm meas}S_{ij}$ are the measured ${\rm sim}S_{ij}$ are the extracted S_{ij}, respectively, while $N_{\rm freq}$ are the number of measured frequency points.

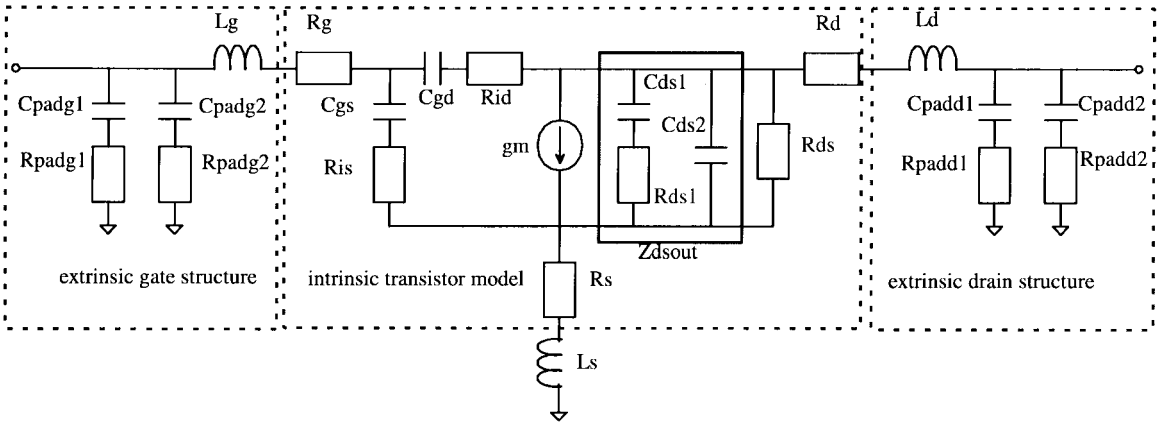

Fig. 1. Small-signal equivalent circuit used for the extraction of the linear intrinsic elements.

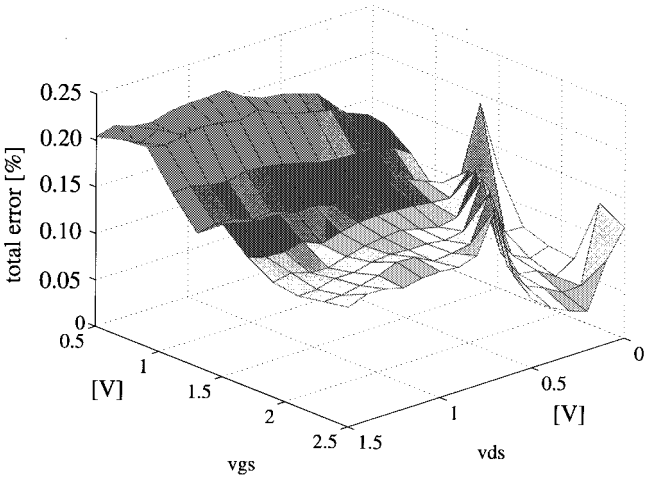

Fig. 2. Total error from (1) between the measured and extracted S-parameters.

Once the equivalent circuit element values of the linear model are known for all bias points, the next challenge is to find equations that fit the extracted capacitances over all bias points. This modeling process is shown in Fig. 3 [11]. The linear parameter extraction yields small-signal equivalent circuit models for each bias point. This data, especially the capacitances, is the input to the nonlinear modeling process along with the dc-current equations of the nonlinear SPICE model. The combination of these elements yields a model for the nonlinear RF performance of a transistor.

III. Improvement for the Nonlinear MOS Model

The model modification consists of new equations for the nonlinear capacitances and the high-frequency output conductance of a MOS transistor. The equations presented are dependent on both the gate–source and the drain–source voltages. A hyperbolic tangent function was chosen to satisfy the shape of the capacitance and resistance curves as a function of the bias voltages. Fig. 4 shows the extracted capacitances $C_{\rm gs}$ as a function of $V_{\rm gs}$ and $V_{\rm ds}$. Since the measured transistors had the bulk connected to the source, the effects of a bulk-source voltage other than zero are not considered.

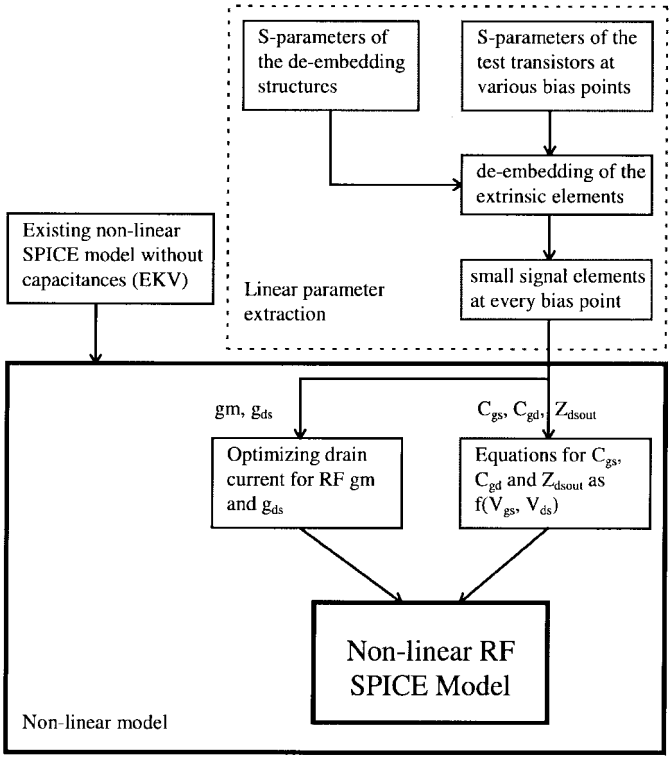

Fig. 3. Flowchart of the modeling process used to obtain nonlinear RF SPICE model.

The equation used for $C_{\rm gs}$ is of the following form:

$$C_{\rm gs} = C_{\rm gs0} + C_{\rm gs1} \cdot \{A_s + B_s \cdot \tanh\cdot[C_s \cdot (V_{\rm gs} - v_t)]\} \cdot \{D_s + E_s \cdot [1 + \tanh\cdot(V_{\rm gs} - V_{\rm ds})] \cdot \tanh\cdot(F_s \cdot V_{\rm ds} - G_s \cdot V_{\rm gs})\} \quad (2)$$

where $C_{\rm gso}$ is a bias independent capacitance, v_t is the threshold voltage, and $C_{\rm gs1}$ is a scaling factor, A_s, B_s, C_s, D_s, E_s, F_s, and G_s are all fit parameters to match this equation to the measured data.

The parameters A_s, B_s, and C_s fit the major curvature as a function of gate–source voltage, while D_s, E_s, F_s, and G_s fit the drain–source dependence. The fit parameters were

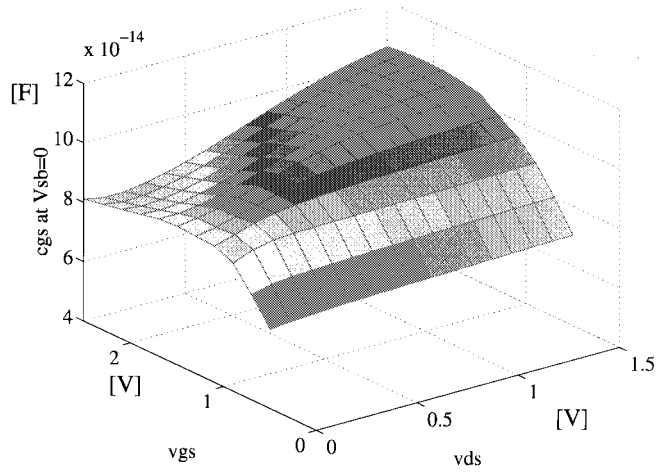

Fig. 4. Extracted gate–source capacitance as a function of $V_{\rm gs}$ and $V_{\rm ds}$ for a transistor of 100-μm gatewidth (20 fingers) and 0.36-μm gate length.

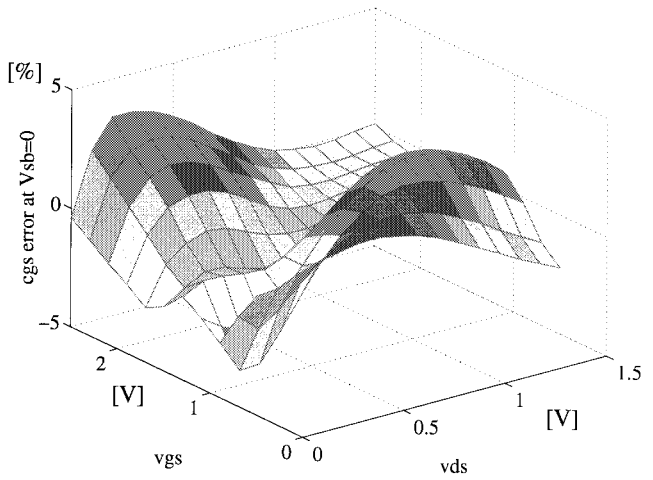

Fig. 5. Normalized difference function from (4) for the gate–source capacitance as a function of bias.

TABLE I
PARAMETER VALUES FOR $C_{\rm gs}$ (2) AND $C_{\rm gd}$ (3) EQUATIONS AS A FUNCTION OF $V_{\rm gs}$ AND $V_{\rm ds}$

Parameter	$C_{\rm gs}$	$C_{\rm gd}$
$C_{\rm gs(gd)0}$	47.1 fF	47.0 fF
$C_{\rm gs(gd)1}$	32.69 fF	32.69 fF
$A_{\rm s(d)}$	1.297	1.247
$B_{\rm s(d)}$	1.0	0.896
$C_{\rm s(d)}$	1.470	1.525
$D_{\rm s(d)}$	0.649	0.630
$E_{\rm s}$	0.122	-
$F_{\rm s}$	0.765	-
$G_{\rm s}$	0.302	-
$v_{\rm t}$	0.643	0.646

optimized by minimizing the mean square error. The values of the fitted parameters for $C_{\rm gs}$ for (2) are shown in Table I.

The same fitting procedure is repeated for the gate–drain capacitance. The equation used for $C_{\rm gd}$ is of the following form:

$$C_{\rm gd} = C_{\rm gd0} + C_{\rm gd1} \cdot \{A_d + B_d \cdot \tanh \cdot [C_d \cdot (-V_{\rm ds} + D_d \cdot V_{\rm gs}) - v_t]\} \tag{3}$$

where $C_{\rm gd0}$ and $C_{\rm gd1}$ are a bias independent capacitance and a scaling factor, respectively, while A_d, B_d, C_d, and D_d are fit parameters and v_t is the threshold voltage. These values are listed in Table I.

To compare the model with the extracted data at each bias point, a difference function was calculated and normalized, as shown in (4). To express the error in percent, the difference function has been multiplied by 100 as follows:

$$\varepsilon_{\rm gs(gd)} = 100 \cdot \frac{{\rm meas}C_{\rm gs(gd)} - {\rm sim}C_{\rm gs(gd)}}{{\rm meas}C_{\rm gs(gd)}}. \tag{4}$$

The normalized difference function, $\varepsilon_{\rm gs}$, for the gate–source capacitance from (4) over the complete bias range is shown in Fig. 5. The maximum difference between simulated and extracted values is less than 5%.

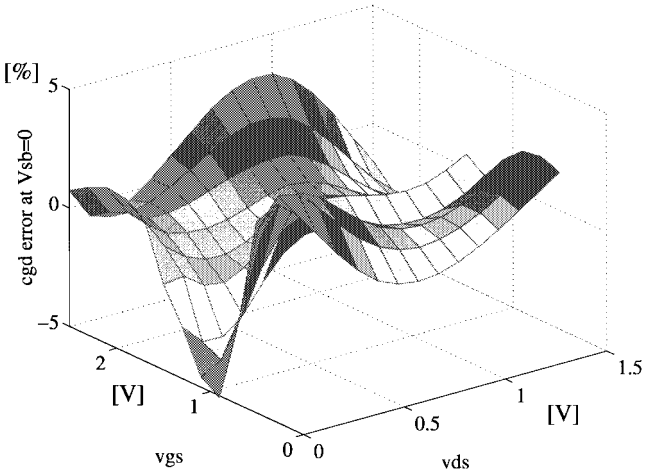

Fig. 6. Normalized difference function from (4) for the gate–drain capacitance as a function of bias.

Using (4), a difference function $\varepsilon_{\rm gd}$ for the gate–drain capacitance can also be calculated. The maximum difference over the measured bias range is also less than 5%, as shown in Fig. 6.

Since the values of $C_{\rm ds2}$, $C_{\rm ds1}$, and $R_{\rm ds1}$ vary only slightly with bias, these elements have all been left constant as a function of bias voltage.

Once the equations for $C_{\rm gs}$, $C_{\rm gd}$, and $Z_{\rm dsout}$ are determined, the implementation in a SPICE-type simulator (in our case, PSpice), is the next step. The interesting region of operation for high frequencies is the saturation region. Thus, this region has first priority when considering the accuracy of the model. For high-frequency models, the most sensitive parameters are the capacitances and g_m [10]. To simplify the implementation, the dc-current equation of the EKV model was used and its g_m and $g_{\rm ds}$ optimized to match the measured dc data, especially in the saturation region. Simultaneously, the dc drain current in this region must also be considered. The nonlinear behavior of the MOS transistor current in all regions of operation is described by 13 EKV parameters [5].

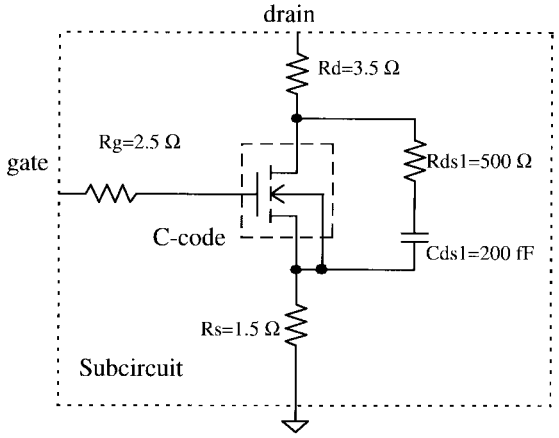

Fig. 7. Schematic of the new model with g_m, $R_{\rm ds}$, $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds2}$ all implemented in C-code, and the series resistances R_g, R_s, R_d, $R_{\rm ds1}$, and $C_{\rm ds1}$ are implemented in a subcircuit.

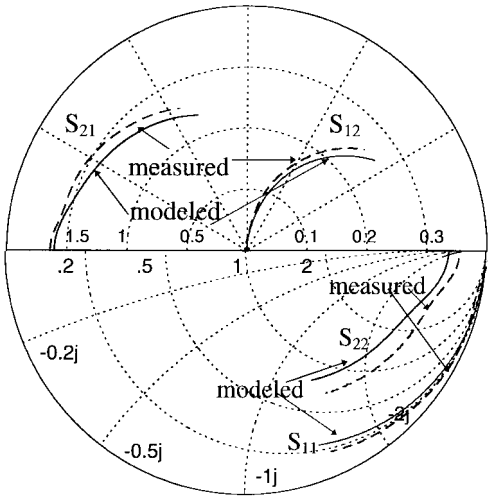

Fig. 8. Measured (dashed) and modeled (solid) S-parameters of a 100-μm-wide gate with 20 fingers at a bias point of $V_{\rm gs} = 1.5$, $V_{\rm ds} = 1.5$, $I_d = 8.3$ mA, and frequency range of 50 MHz to 10 GHz. Note the different scale for S_{12} and S_{21}.

The proposed equations for the nonlinear capacitances were implemented within the model C-code.[3] Our experience has shown that the implementation in C-code increases the accuracy and simulation speed while reducing convergence problems caused by subcircuit implementation [11]. Since the new model assumes the bulk–source voltage to be zero, only two capacitances are visible at the gate ($C_{\rm gs}$ and $C_{\rm gd}$). Thus, the capacitance part of the new MOSFET model differs only slightly from the Statz GaAs FET model in SPICE. The implementation of gate–source and gate–drain capacitance is well explained in [12] for this model. The new capacitances are similarly implemented as those of the Statz model, and are charge conserving. The new SPICE model (see Fig. 7) consists of two new equations for the internal capacitances $C_{\rm gs}$ and $C_{\rm gd}$, in addition to the EKV current equations and a constant $C_{\rm ds2}$. The nonlinear current source of the EKV transistor model provides the g_m, $g_{\rm ds}$ for the dc-current characteristics. $R_{\rm ds1}$ and $C_{\rm ds1}$ and the series resistances R_g, R_s, and R_d were added in a subcircuit.

By combining and implementing new capacitance equations and EKV dc equations, a new model has been developed for RF simulations of MOSFET's.

IV. Results

A. Bias-Dependent S-Parameters

The simulations of the implemented high-frequency MOSFET model have shown very good agreement with the measurements over a wide range of bias points. The model is valid up to 10 GHz, as can be seen by comparing the simulation and the measurements of all S-parameters at a typical bias point (Fig. 8). The transistor with a gatewidth of 100 μm (20 fingers) and a gate length of 0.36 μm was biased at a $V_{\rm gs} = V_{\rm ds} = 1.5$ V and $I_d = 8.3$ mA.

Since the output conductance is determined by the derivative of the dc drain current, a fairly large difference is seen in the output reflection (S_{22} in Fig. 8). Such differences could be reduced with a more careful determination of the dc-current model parameters.

[3] *PSpice Manual Tutorial, Applicat. Notes, and Design Ideas.*Microsim Corporation, Irvine, CA, 1995.

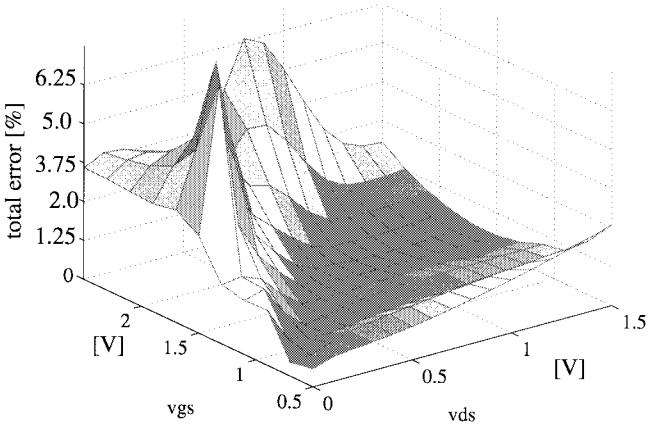

Fig. 9. Total error from (1) between the measured and simulated S-parameters of the new model. The g_m, $R_{\rm ds}$, and I_d are derived from the dc-current equation.

A total error function between the S-parameters of the model and the measurements was defined in (1). The error function is similar to the square error function except that the individual errors have been normalized to weight each of the S-parameters equally. All measured bias points were simulated. The error is calculated at each bias point and given in percent. The total error (1) for all measured bias points between the measured and the simulated S-parameters of the new model is shown in Fig. 9.

When the extracted model is transformed into a large-signal model and implemented in PSpice, a few approximations were made. Both the g_m and $r_{\rm ds}$ are not derived from the high-frequency extractions. These elements are calculated from the derivatives of the dc drain current. Thus, the total error is slightly larger than the extraction error (see Fig. 2) due to the approximations. At supply voltages of 2.7 V and for operation

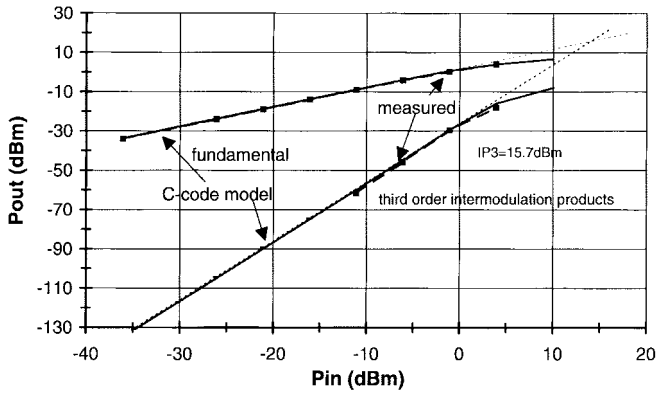

Fig. 10. Measured (squares) and simulated in C-code (solid lines) two-tone IM products at frequencies of 1.8, 1.805 GHz, and a bias point of $V_{\rm gs} = 1.6$ V, $V_{\rm ds} = 2.0$ V, and $I_d = 10.68$ mA.

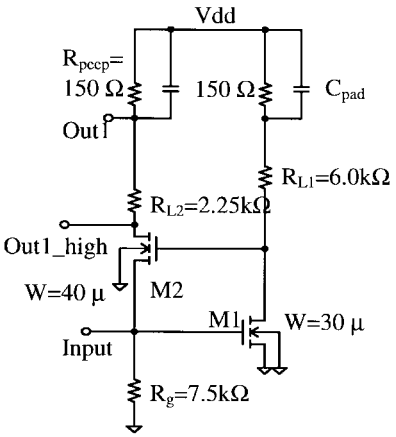

Fig. 11. Circuit schematic of the broad-band amplifier with measured resistor values.

in the saturation region, the gate and drain voltages of a single transistor are usually below 1.5 V where the total error is less than 1%.

B. Intermodulation Prediction

To test the nonlinear performance of the new model, the two-tone intermodulation (IM) products of a transistor were measured and simulated. The input frequencies were chosen to be in the frequency range of interest for CMOS telecommunication applications (1.8 GHz). The third-order IM products of a transistor with a total gatewidth of 100 μm split into 20 fingers and a gate length of 0.36 μm were measured at a bias point of $V_{\rm gs} = 1.6$ V, $V_{\rm ds} = 2.5$ V, and $I_d = 10.68$ mA. As shown in Fig. 10, the simulations (solid lines) correspond well to the measured (dotted lines with squares) third-order IM products. The two curves are practically identical, indicating an excellent agreement between model and measurement.

C. Circuit-Level Simulations

To further test the new model, a simple amplifier [13] has been designed and measured. A circuit schematic of the amplifier is shown in Fig. 11. Due to the feedback transistor, the input impedance of this amplifier is low. The input impedance at low frequencies is determined by the transconductance of transistor $M2$ and the gain of the loop including transistor $M1$.

The input impedance and voltage gain for the amplifier at low frequencies have been calculated with a very simple small-signal model consisting of $C_{\rm gs}$ and g_m [14]. The input admittance at dc is given in (5)

$$Y_{\rm in} = \frac{1}{R_g} + g_{m\,M2} \cdot [1 + g_{m\,M1} \cdot (R_{L1} + R_{\rm peep})]. \quad (5)$$

The voltage gain from the input to Out1_high at low frequencies can be calculated using (6)

$$A_v = g_{m\,M2} \cdot (R_{L2} + R_{\rm peep}) \cdot [g_{m\,M1} \cdot (R_{L1} + R_{\rm peep})]. \quad (6)$$

In order to facilitate measurements in a 50-Ω environment, peep resistors were placed between the various load resistors and the supply voltage V_{dd}. These resistors are 150 Ω and are directly accessible via bonding pads for measurements.

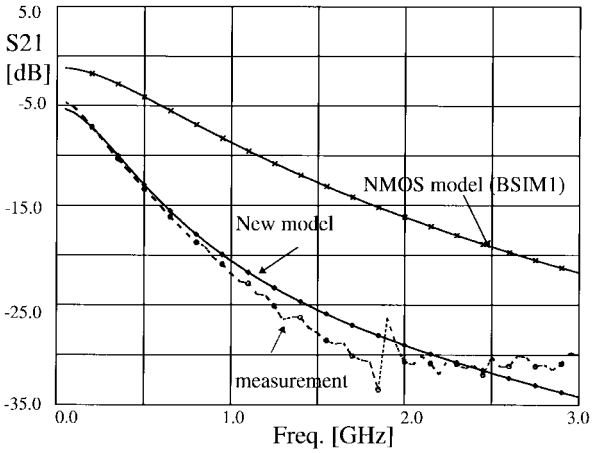

Fig. 12. Measured (dotted line) and simulated S_{21} in decibels of the broad-band amplifier using the measured resistance values.

Thus, the frequency performance of the amplifier at the high-impedance node is not degraded by the bonding pad. Yet, the performance of the amplifier can still be calculated for the higher internal impedances from the measured output voltage at Out1 using the well-known equations for a capacitively loaded resistive divider.

The resistors are made of high-resistivity n-diffused material such that the small resistors track with the larger resistors. However, to obtain large values for the load resistors, the width of the diffusion resistors was rather small, causing these values to be sensitive to process variations. Resistors measured on the process control monitor have measured 150 Ω. All measurements and simulations have been performed with measured resistor values shown in Fig. 11.

The simulated dc-bias points were very close to the measured dc-bias points, as shown in Table II. The supply voltage V_{dd} in the dc simulation was set to the measured value.

The measured and simulated S_{21} parameter of the amplifier is shown in Fig. 12. The new model shows good agreement with the measured data. As a comparison, the same circuit has been simulated with a standard BSIM1 [3] model (NMOS model). This simulation predicts almost 10 dB more gain at 1 GHz than actually measured.

TABLE II
MEASURED AND SIMULATED BIAS VOLTAGES OF THE AMPLIFIER

	Simulated	Measured
Input	0.8126 V	0.7945 V
Out1	4.0348 V	4.0346 V
V_{dd}	4.0514 V	4.0514 V

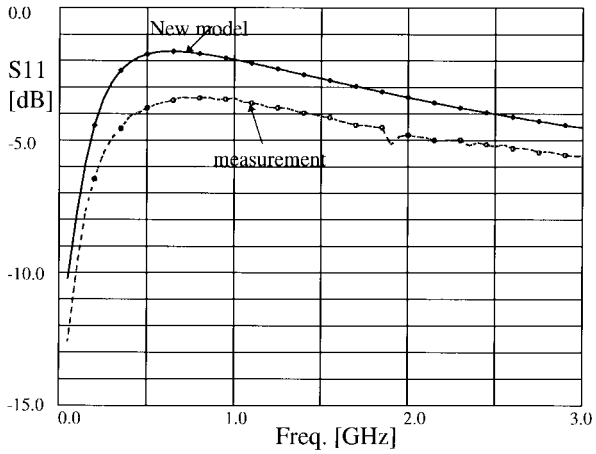

Fig. 13. Measured (dotted line) and simulated input reflection S_{11} in decibels of the broad-band amplifier.

The measurements were performed at Out1 (Fig. 11) and may be calculated back to the high-impedance output Out1_high. To determine the high-impedance voltage gain, 24 dB can be added to the results in Fig. 12. Thus, this amplifier has approximately 19 dB of voltage gain and a -3-dB bandwidth of approximately 200 MHz.

The measured and simulated input reflection S_{11} of the amplifier is shown in Fig. 13. The measurement is approximately 2 dB lower than the simulations with the new model. As was verified by a qualitative test, this difference may be attributed to the bulk-source effect of transistor $M2$, which is not included in our model.

It is shown in Fig. 14 that the measured and simulated output reflection S_{22} using the new model match very well at frequencies up to 2 GHz. At frequencies above 2.2 GHz, the measured S_{22} deviates from the predicted S_{22} values due to a resonance of the measurement setup.

As the results have shown, the new model predicted the S-parameters of this amplifier with good accuracy.

Only the input return loss S_{11} showed a difference that can be attributed to the bulk effect not included in the model. The model is sufficiently accurate when considering common source stages; however, when simulating common gate or source follower stages, an additional bulk node must be added.

V. CONCLUSIONS

A nonlinear high-frequency MOSFET model has been developed for frequencies up to 10 GHz. The model is based on S-parameter measurements at various bias points. The microwave frequency performance of the model has been investigated concerning the bias dependence, IM performance, and circuit simulation. The simulations and measurements show good agreement over a wide range of bias voltages. At

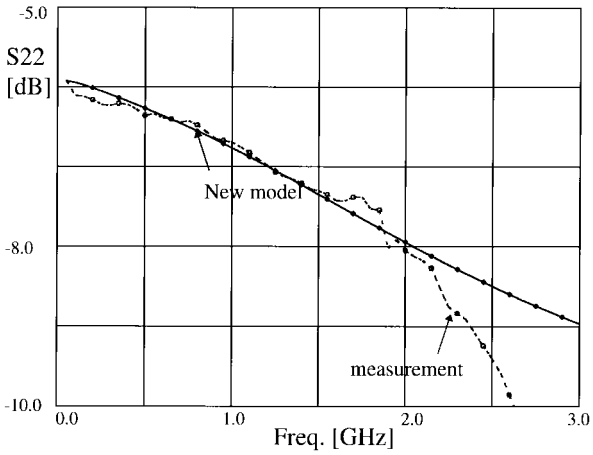

Fig. 14. Measured (dotted line) and simulated S_{22} in decibels of the broad-band amplifier using $R_{\rm peep} = 150\ \Omega$.

a supply voltage of 2.7 V, and for operation in the saturation region, the gate and drain bias voltages of a single transistor are usually below 1.5 V. The difference in this region of operation between measured and simulated S-parameters of the new model is less than 1%. As was shown with the third-order IM simulations, the nonlinear behavior is also well predicted. By implementing the new MOSFET model in C-program code, simulation accuracy has been increased while convergence problems have been eliminated. The simulation speed is considerably improved over the previously used subcircuit model [11] such that simulations of large circuit are now possible. As presented in this paper, these modifications significantly improve prediction of the high-frequency performance of a simple amplifier over a standard BSIM1 NMOS model. Thus, a versatile model with less than 20 model parameters, good performance in all regions of operation [4], [5], and good RF performance is presented.

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